

Guest Editorial

Special Section on Application Specific Processors

PROCESSORS, today, are everywhere, doing far more than providing the computational power of your laptop. Tens or even hundreds of processors these days populate your house and are at the heart of objects as diverse as your car, your cell phone, your broadband modem, your high-definition television, and your camera. With the current numbers of transistors available on typical VLSI dies, processors are rapidly becoming the keystone of system design: single chips may contain several of them, ranging from extremely simple pipelines to complex superscalar engines, and responsible of individual subsystems and functionalities such as specific wireless protocols, given flavors of complex encoding and decoding, advanced multimedia real-time data processing, as well as rich user interfaces. Processors are quickly displacing dedicated application-specific circuitry in many applications because they can more easily accommodate new and more articulate functions, such as modern high-quality coding techniques; also, they provide much needed flexibility for systems which implement standards that may not even yet exist at the time of design—processors represent a very solid and well-understood design paradigm which has critically contributed to the development of electronics in the last decades. Yet, these processors are very different from your traditional superscalar out-of-order processor and even from textbook RISC engines: these small processor subsystems often need leading-edge performance for their applications but cannot afford more than a fraction of the area and energy cost of general purpose computing devices. Designers can only achieve that through specialization of the processor subsystems to the application domain they must serve. The heterogeneity of the processor subsystems which populate your house is flabbergasting.

We are very pleased to present this Special Section on Application Specific Processors, dedicated to leading research issues on how such adaptation to the application domain can be achieved with acceptable design effort. This section consists of eight articles, four of which are extended versions of papers presented at the Fifth Workshop on Application Specific Processors (WASP) held in 2007. The success of this workshop was one of the strong motivations and reasons for creating this special section. WASP has been for a few years a small but thriving venue where edge research issues in processor specialization have been discussed; it has now evolved into the larger IEEE Symposium on Application Specific Processors (SASP) which

co-located with the Design Automation Conference in 2008. For this section, we have distilled the best of a few dozen submissions, which either were in turn among the best of those presented at the workshop or were submitted in response to an open call for papers. Each manuscript underwent a rigorous review process following the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (TVLSI) review standards, with accepted papers undergoing up to three review cycles. Finally, eight papers were selected to be included in the special section and four additional papers will be published in regular TVLSI issues. We wholeheartedly thank all of the reviewers and the Editor-in-Chief for their invaluable help in making this Special Section a reality.

The first two papers of this Special Section address design automation issues related to the automatic specialization process. The first article, “Recurrence-Aware Instruction Set Selection for Extensible Embedded Processors” by Bonzini and Pozzi, describes a novel methodology for automated instruction set extension that comprehensively addresses operation recurrence. In “Outer Loop Pipelining for Application Specific Datapaths in FPGAs,” Turkington *et al.* have adapted a loop transformation technique to speed up application specific FPGA coprocessors derived from software descriptions. The use of FPGAs in the latter paper bring us to the next set of contributions, related to the introduction of reconfigurable lattices in processors to achieve flexibility at unprecedented levels of performance and efficiency. The paper “A Design Flow for Architecture Exploration and Implementation of Partially Reconfigurable Processors” by Karuri *et al.* describes an extended architecture description language and a methodology for design space exploration and automatic generation of reconfigurable application specific processors. In “Efficient Resource Utilization for an Extensible Processor Through Dynamic Instruction Set Adaptation,” Bauer *et al.* address the problem of allocating dynamically configurable resources for instruction set adaptation. The next paper, “A Reconfigurable ASIP for Convolutional and Turbo Decoding in an SDR Environment” by Vogt and Wehn, transitions to the third and last part of this section, dedicated to applications of specialized processors; this paper presents a family of weakly-programmable application specific instruction-set processors that are strongly fine-tuned to software-defined radio decoding tasks. The next paper, “High Performance Architecture of an Application Specific Processor for the H.264 Deblocking Filter” by Dang, introduces an efficient and high-performance

application specific processor architecture to implement an important part of the H.264 video compression standard. After software radios and video, “A Processing Path Dispatcher in Network Processor MPSoCs,” by Ohlendorf *et al.*, presents a solution to a multi-field packet classification problem that is used for optimized packet assignment to different data paths within a network processor SoC. Last, but not least, in “Automatic Processor Customization for Zero-Overhead Online Software Verification,” Lu and Forin show a very different application of processor specialization, that is, the automatic extension of a processor with hardware for no-overhead verification of the software it runs.

We hope that you will enjoy this Special Section at least as much as it was a pleasure for us to put it together. Have a nice reading!

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Paolo Ienne (S'90–M'96) received the Dottore degree in electronic engineering from the Politecnico di Milano, Milan, Italy, in 1991, and the Ph.D. degree from the Ecole Polytechnique Fédérale de Lausanne (EPFL), Lausanne, Switzerland, in 1996.

In December 1996, he joined the Semiconductors Group of Siemens AG (which later became Infineon Technologies AG), Munich, Germany, where, after working on datapath generation tools, he became the Head of the Embedded Memory Unit, Design Libraries Division. Since 2000, he has been with the School of Computer and Communication Sciences, EPFL, where he is currently a Professor and the Head of the Processor Architecture Laboratory. His research interests include various aspects of computer and processor architecture, computer arithmetic, reconfigurable computing, and multiprocessor systems-on-chip.

Dr. Ienne was a recipient of the DAC 2003 and the CASES 2007 Best Paper Awards. He is or has been a member of the program committees of several international conferences and workshops, including Design Automation and Test in Europe (DATE), the International Conference on

Computer Aided Design (ICCAD), the International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), the International Symposium on Low Power Electronics and Design (ISLPED), the International Symposium on High-Performance Computer Architecture (HPCA), the International Conference on Field Programmable Logic and Applications (FPL), and the IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC). He has been a Program Cochair of the Fifth Workshop on Application Specific Processors (WASP'07) and General Cochair of the Sixth IEEE Symposium on Application Specific Processors (SASP'08).



Peter Petrov received the B.S. and M.S. degrees in computer science from Sofia University, Sofia, Bulgaria, in 1998, and the Ph.D. degree in Computer Engineering from the University of California, San Diego, in 2004.

In July 2004, he joined the with the Electrical and Computer Engineering Department, University of Maryland, College Park, where he is currently an Assistant Professor. His research work covers broadly the areas of low-power and real-time embedded systems and more specifically application-specific embedded processors, multiprocessors, and systems. He is one of the founders of the Workshop on Application Specific Processors (WASP) and has served as a General and Program Chair of this annual event. He is a founding member and a General Cochair of the Sixth IEEE Symposium on Application Specific Processors (SASP'08), which was co-located with the Design Automation Conference in 2008. He has served as a technical program member of the Symposium on Integrated Circuits and Systems (SBCCI) and the International Conference on Computer Design (ICCD).